

CLAIMS:

What is claimed is:

1 1. An interface circuit for interfacing a system
2 controller integrated circuit and a plurality of
3 peripheral integrated circuits, said interface circuit
4 comprising:

5 a node within said system controller integrated
6 circuit commonly connected to a first and a second one of
7 said plurality of peripheral integrated circuits;

8 first switch means for selectively connecting said
9 node to a first circuit of the systems controller
10 integrated circuit for communicating signals with
11 reference to said first peripheral integrated circuit;

12 second switch means for selectively connecting said
13 node to a second circuit of the systems controller
14 integrated circuit for communicating signals with
15 reference to said second peripheral integrated circuit;

16 signal means for early enabling and late disabling of
17 said first and second switch means consistent with setup
18 and hold times of the respective first and second
19 peripheral integrated circuits.

1 2. The interface circuit of Claim 1, wherein said
2 node is an output pin for providing an output signal to
3 said first one and said second one of said plurality of
4 peripheral integrated circuits, and wherein said first
5 switch means comprises a selector within said system
6 controller integrated circuit having a select input
7 coupled to signal means.

1 3. The interface circuit of Claim 2, wherein said first
2 peripheral integrated circuit is a memory device, said
3 second peripheral integrated circuit is a bus controller,
4 said first circuit is an address generator and said second
5 circuit is a bus control generator.

1 4. The interface circuit of Claim 2, wherein said first
2 circuit is a data signal generator and said second circuit
3 is an address generator.

1 5. The interface circuit of Claim 2, wherein said first
2 switch means comprises a tri-state buffer having an input
3 coupled to said first circuit, an output coupled to said
4 node, and an enable input coupled to said signal means;
5 and wherein said second switch means comprises a second
6 tri-state buffer having an input coupled to said second
7 circuit, an output coupled to said mode, and an disable
8 input coupled to said signal means.

1 6. The interface circuit of Claim 2, wherein said first
2 and said second switch means comprise:

3 a multiplexer having inputs coupled to said first
4 circuit and said second circuit and a select input coupled
5 to said signal means; and

6 an output driver having an input coupled to an output
7 of said multiplexer and an output coupled to said node.

1 7. The interface circuit of Claim 1, wherein said node is
2 an input pin for receiving a first signal from said first
3 peripheral integrated circuit and a second signal from
4 said second peripheral integrated circuit.

1 8. The interface circuit of Claim 7 further comprising:

2 first chip select signal means coupled to said first
3 peripheral integrated circuit for enabling communication
4 with said first peripheral integrated circuit;

5 second chip select signal means coupled to said
6 second peripheral integrated circuit for enabling
7 communication with said second peripheral integrated
8 circuit, and wherein said first circuit comprises a first
9 transparent latch having a gate input coupled to said
10 first chip select signal means, whereby a state of said
11 node may be maintained at said first circuit when said
12 signals means deselects communication said first
13 peripheral integrated circuit, and wherein said second
14 circuit comprises a second transparent latch having a gate
15 input coupled to said second chip select signal means,
16 whereby a state of said node may be maintained at said
17 second circuit when said signal means deselects said
18 second peripheral integrated circuit.

1 9. The interface circuit of Claim 1, wherein said node is
2 a pin for receiving a first signal from said first
3 peripheral integrated circuit and transmitting a second
4 signal to said second peripheral integrated circuit, and
5 wherein said second switch means comprises a
6 tri-state buffer having an enable input coupled to said
7 signal means an output coupled to said node and an input
8 coupled to said first circuit.

1 10. The interface circuit of Claim 9, wherein said first
2 circuit comprises a transparent latch having a gate input
3 coupled to said signal means, whereby a state of said node
4 may be maintained when said signal means disables said
5 gate input.

1 11. The interface circuit of Claim 1, wherein said node is
2 a bi-directional interface pin for interfacing
3 bidirectional signals to said first and said second
4 peripheral integrated circuits, wherein said first circuit
5 and said second circuit include bidirectional input/output
6 connections, wherein said first switch means comprises a
7 transmission gate having a select input coupled to said
8 signal means, a first terminal connected to said node and
9 a second terminal coupled to said first circuit, and
10 wherein said second switch means comprises a transmission
11 gate having a select input coupled to said signal means, a
12 first terminal connected to said node and a second
13 terminal coupled to said second circuit.

1 12. A method for coupling a plurality of signals of
2 differing types between a plurality of peripheral
3 integrated circuits and a system controller integrated
4 circuit, said method comprising:

5 generating a peripheral select signal within said
6 system controller integrated circuit for early enabling
7 and late disabling switch means consistent with setup and
8 hold times of the peripheral integrated circuits;

9 generating a chip select signal from said peripheral
10 select signal;

11 supplying said chip select signal to a corresponding
12 peripheral integrated circuit chip select input;

13 selecting one of a plurality of internal signals
14 each associated with one of said plurality of peripheral
15 integrated circuits in conformity with said peripheral
16 select signal; and

17 coupling said selected internal signal to an external
18 pin connected to each of said plurality of peripheral
19 integrated circuits, whereby said selecting and said
20 coupling interface a internal signal associated with a
21 peripheral integrated circuit corresponding to said chip
22 select signal.